UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/595,860	06/16/2000	Jorg Berthold	GR-97-P-6457	2756

7590 03/19/2003

Lerner & Greenberg P A
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER
NGUYEN, CUONG QUANG

ART UNIT	PAPER NUMBER
2811	19

DATE MAILED: 03/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/595,860	BERTHOLD ET AL.	
	Examiner	Art Unit	
	Cuong Q Nguyen	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24,27 and 28* is/are pending in the application.

4a) Of the above claim(s) *24 and 28* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 1 and 17 are objected to because of the following informalities:

In claim 1 line 31, the term "isolation layer" should be changed to "insulation layer".

In claim 27 line 3, the term "isolation layer" should be changed to "insulation layer"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 2, the expression "a diffusion barrier.....disposed at least on of a surface of contact holes and said connection pieces." is unclear. It is unclear that first or second contact holes the "contact holes" is implied to.

In claim 20, the expression "the further diffusion blocker prevents bulk outdiffusion of copper into said insulation layer." is unclear. It is unclear that first or second insulation layer the "insulation layer" is implied to.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-7, 18-23 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. (US 5,935,766) in view of Cohen et al. (US 5,679,269) and further in view of Bothra et al. (US 5,798,559).

Regarding claims 1, 3- 6, Cheek et al. discloses an integrated circuit comprising: a plurality of structure planes on which the metalizations are formed; the structure planes including an element structure plane (a substrate 100); electrically active elements formed on the element structure plane; a first insulation layer (130, a semiconductor oxide layer. Col.6 lines 12-19) formed above the element structure plane, the first insulation layer having first contact holes filled with a metal (140, 142, 144); a second insulation layer (160) formed above the first insulation layer, the second insulation layer having second contact holes and filled with W electrical connecting leads (190, 192, 194) (col.7 lines 5-15); connection pieces (Al metal-1 layers 150, 152, 154. Col.6, lines 35-40) formed underneath the electrical connecting leads and covering the first contact holes and contacting the connection leads; the connection pieces are covered by the second insolation layer (160). See Cheek et al.'s Fig.1N.

Cheek et al. does not teach that at least one diffusion blocker layer formed between first and second insulation layers and underneath the electrical connecting leads, wherein the diffusion blocker is interrupted only in a region having first contact holes and the connection pieces covering the contact hole. Cheek et al. also does not teach that the second contact holes are filled with copper in a whole-area manner.

Cohen et al. discloses an integrated circuit comprising: a contact hole (45) is filled with W or Cu (col.6, lines 10-15) an a whole-area manner. See Cohen et al.'s Fig.3.

Bothra et al. discloses an integrated circuit comprising: a silicon nitride diffusion blocker layer (116) (col.4 lines 50-55) formed between first and second insulation layers and underneath electrical connecting lead (134), wherein the diffusion blocker is interrupted only in a region having first contact holes (114, 110) and connection pieces (118) covering the contact hole. See Bothra et al.'s Fig.3K.

It would have been obvious to one of ordinary skill in the art to fill the second contact holes of Cu instead of W as taught by Cohen et al. in Cheek et al.'s device because Cu and W are art recognized material for filling the contact holes in the semiconductor integrated circuit and they are interchangeable. It also would have been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layer as taught by Bothra et al. into Cheek et al.'s device in order to prevent the moisture that cause corrosion or contaminants to reach the semiconductor substrate. See Bothra et al.'s col.4 lines 52-60.

It is noted that the diffusion blocker layer is formed of silicon nitride which is identical as material for forming the diffusion blocker layer in the present invention. So, it is inherent that the diffusion blocker layer in above device can be impeding and preventing a diffusion copper as claimed.

Regarding claims 2, 18, 19, 20, Cheek et al. further that a Ti/TiN layer (a further diffusion blocker) formed on a surface second contact holes (col.7 lines 5-15). It is inherent that, when one of ordinary skill in the art fills the second contact holes of Cu, the Ti/TiN layer can function as a diffusion barrier layer impeding the Cu in the second contact holes to prevent bulk outdiffusion of Cu into the second insulating layer.

Regarding claim 27, in the above device being formed by the combination of Cheek et al., Cohen et al. and Bothra et al., the blocker layer is inherently including an upper surface facing the second insulation layer and a lower surface facing the structure plane and connection pieces being in contact with upper surface of the blocker layer.

Regarding claim 7, Bothra et al. does not explicitly teach that silicon nitride blocker is a Si3N4.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of Si3N4 as claimed because silicon nitride is commonly Si3N4.

Chiang et al. discloses an integrated circuit comprising: silicon nitride diffusion blocker layers (323, 390, 392) having a thickness in the range of 30 nm to 150 nm (Chiang et al.'s col.15, lines 17-22) formed between each of a plurality of structure

planes, wherein the diffusion blocker layer is interrupted only in a region having contact holes and the connection pieces covering the contact hole. See Chiang et al.'s Fig.25.

Regarding claims 21-23, Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above. However, these references do not teach that the blocker layer has a thickness greater than a thickness of the further blocker so that. a diffusion through the blocker layer is less than 10% of a diffusion through the further diffusion blocker.

It is known in the art that the diffusion through the blocker layer is depending on the thickness of the blocker.

Therefore, it would have been obvious to one of ordinary skill in the art to form the blocker layer having a thickness greater than the thickness of further blocker layer so that the diffusion through the blocker layer is less than 10% of a diffusion through the further diffusion blocker as claimed because the thickness of blocker layers are art recognized variable of importance which are subject to routine experimentation and optimization.

Claims 8, 9, and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Chiang et al. (US 5,739,579).

Regarding claims 8, 9, Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above. However, Bothra et al. does not teach that the blocker layer formed of SiON.

It is conventional and also taught by Chiang et al. that SiN and SiON are art recognized material for forming the blocker layer (etch-stop layer) in an integrated circuit and they are interchangeable. See Chiang et al.'s col.14, lines 65-67.

Therefore, it would have been obvious to one of ordinary skill in the art to form the blocker layer of SiON instead of SiN as taught by Chiang et al.

Regarding claim 14, Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above. However, Bothra et al. does not teach that the blocker layer has a thickness of between 50 nm and 800 nm.

Chiang et al. further teach that the silicon nitride diffusion blocker layers (323) having a thickness in the range of 30 nm to 150 nm (Chiang et al.'s col.15, lines 17-22). See Chiang et al.'s Fig.25.

It would have been obvious to one of ordinary skill in the art to provide the blocker layer having the thickness as taught by Chiang et al. because the thickness of blocker layer is an art recognized variable of importance which is subject to routine experimentation and optimization.

Regarding claims 15 and 16, Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above.

However, these references do not teach that blocker layer are disposed on different ones of structure planes.

Chiang et al. further teaches that silicon nitride diffusion blocker layers (323, 390, 392) formed between each of a plurality of structure planes. See Chiang et al.'s Fig.25.

It would have been obvious to one of ordinary skill in the art to incorporate the silicon nitride blocker layers between the structure planes as taught by Chiang et al. into Cheek et al.'s device in order to prevent electrical shorting. Chiang et al..'s col.15, lines 4-15.

Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of Hong (US 6,008,117).

Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above but fail to teach that the blocker layer is formed of metal oxide such as TiO2.

Hong discloses an integrated circuit comprising a blocker layer (14) is formed of silicon nitride or TiO2. See Hong's Fig.1H and col.2 lines 52-56.

It would have been obvious to one of ordinary skill in the art to form the blocker layer of TiO2 instead of silicon nitride as taught by Hong because materials such as

silicon nitride, and TiO2 are art recognized materials for forming the blocker layer in the semiconductor device and they are interchangeable.

Claims 10 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. in view of Cohen et al., Bothra et al. and further in view of McCollum et al. (US 5,552,627).

Cheek et al., Cohen et al. and Bothra et al. substantially teach all the limitation of claims 1-7, 18-20 and 27 as shown above but fail to teach that the blocker layer is formed of a fluorinated nitride such as fluorooxynitride.

McCollum et al. discloses an integrated circuit comprising a blocker layer formed of fluorinated nitride material by deposited the silicon nitride using an NF3 atmosphere in the reactor. McCollum et al. teaches that fluorinated nitride has a lower leakage than a similar nitride material. See McCollum et al.'s Fig.3 and col.8, lines 42-51.

Therefore, it would have been obvious to one of ordinary skill in the art to form the block layer of silicon nitride or silicon oxynitride by deposited the silicon nitride using an NF3 atmosphere as taught by McCollum et al. in order to reduce the leakage of the blocker layer.

It is inherent that the silicon oxynitride is formed by deposited the silicon nitride using an NF3 atmosphere would produce fluorinated nitride such as fluorooxynitride.

R spons to Arguments

4. Applicant's arguments with respect to claims 1-23 and 27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

6. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should be directed to the Technology Center Receptionists whose telephone number is 308-0956.

Cuong Nguyen

Primary examiner

March 13, 2003